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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,437	03/20/2001	Dagnachew Birru	US010069	9839

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EXAMINER	
GOSHTASBI, JAMSHID	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/812,437	BIRRU, DAGNACHEW	
	Examiner	Art Unit	
	Jamshid Goshtasbi-G.	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are pending in the application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites (line 15) the limitation "said number." There is insufficient antecedent basis for this limitation in the claim. Also, there is insufficient antecedent basis for the recited (line 16) limitation "said filter coefficient +1/-1 or zero." Further, the terms " greater " and "less" in claim 1 are relative terms which render the claim indefinite. The terms "greater" and "less" are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Speed and redundancy have been rendered indefinite by the use of "greater" and "less" in "a greater speed with less redundancy" (line 27).

Claim 5 recites (line 1) the limitation "said inverter circuit" in Claim 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites (line 1) the limitation "said determined number" in Claim 2. There is insufficient antecedent basis for this limitation in the claim.

As to **Claim 12**, the terms " greater " and "less" in claim 1 are relative terms which render the claim indefinite. The terms "greater" and "less" are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. Speed and redundancy have been rendered indefinite by the use of "greater" and "less" in "a greater speed with less redundancy" (lines 20-21).

Claim 17 recites (line 2) the limitation "said adding step e)" in Claim 13. There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites (lines 7-8) the limitation "said determined number." There is insufficient antecedent basis for this limitation in the claim.

Claims 2-4, 6-10, 13-16 and **19** are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1,12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Lemonds et al. (US 6611857 B1).

As to **Claim 1**, Applicant's admitted prior art (Fig. 2; Page 3, lines 1-6) discloses a typical implementation of a hardware unit of a feedback path FIR filter (of a DFE) for carrying out a second term summation in the convolution operation, where the N-bit filter coefficients g_n (p. 3, line 20) and the input symbols y_n (a plurality of discrete digital values; p. 3, line 15) are multiplied by a multiplies and the result is stored and added by an adder to the previous value (result) stored in an accumulator register; further, for an 8-level input symbol (when represented as 4-bit two's complement number), the conventional implementation required the use of a 4×N-bit multiplier (p. 4, lines 4-5) usually used in combination with an accumulator; Applicant's admitted prior art, however, fails to teach the multiplier device in any further details; however, Lemonds et al. discloses comprising a multiplier and a set of filter coefficients (Fig. 1; col. 2, lines 35-37) for performing convolution on an input data, which includes multiplying the input data by coefficients (col. 2, lines 62-65); further, Lemonds et al. teaches the multiplier comprises an encoder for optimizing the performance of the multiplier by utilizing a modified radix-4 Both algorithm for multiplying the inputs (col. 3, lines 38-41); further, the encoder (decoder) is for receiving the (binary code representing the plurality of the discrete digital level values) input data (col. 4, lines 29-30) and generating (control signals for generating) a plurality of partial products (intermediate multiplication results) based on specified bits of one of the inputs (col. 3, lines 38-45), and that the generated partial products (intermediate multiplication results) may be added together to generate the (final) multiplication result. Therefore, it would have been obvious to one of ordinary skill in the art at

the time the invention was made to incorporate the teachings of Lemonds et al. into the method of Applicant's admitted prior art for producing the claimed invention because incorporating a Booth's like encoder into the multiplier provides for optimization of the multiplication (reducing the circuit complexity and increasing the multiplication speed) by utilizing a modified (as needed) well known Booth algorithm to generate intermediate multiplication results by performing a series simple operations (on the multiplicand, the filter coefficients) including negation (inverting the bits, by using exclusive OR gates, for instance; i.e., multiplication by -1), multiplication by 0 (that can be done by ANDing the bits logic "0"), multiplication by –1(by ANDing the inverted bits with logic "1"), multiplication by powers of 2 (by shifting to the left) to effect the multiplication of the multiplicand by a power of two (such as discrete digital values 4 and 8 as needed), and ADDing the intermediate multiplication result together (using any of the well known techniques for adding binary signed numbers and storing the result in an accumulator) for producing the final multiplication result, where implementing the encoder (decoder) logic that generates control signals based on the detected input binary code (representing the value associated with each of the plurality of the discrete digital level values) is a well known practice in the art.

As to **Claim 12**, the claimed method for performing multiplication recites features that correspond with subject matter mentioned above in the rejection of Claim 1 and are applicable hereto.

Claims 2-11, 13-15, and 17 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Applicant's admitted prior art in view of Lemonds et al. (US 6611857 B1) as applied to Claim 1 above, and further in view of Tan et al. (US 6226323 B1), Davis (US 5957999).

Claim 2 inherits all the limitations of Claim 1; further, both Applicant's admitted prior art and Lemonds et al. fail to teach representing the input data (multiplier) of the as a 3-bit code; however, Tan et al. discloses a technique for minimizing decision feedback equalizer word length and teaches (Fig. 21; col. 23, lines 9-15) the 8 possible levels (+7/-7, +5/-5, +3/-3, and +1/-1) in a 8-VSB standard DTV system (error signal) are represented by a three (3)-bit code. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tan et al. into the method of Applicant's admitted prior art (in view of Lemonds et al.) for producing the claimed invention because it provides with a minimal (3-bit) binary code (needed for) representing the 8 discrete digital level values at the input of the encoder of the multiplier.

Claim 3 inherits all the limitations of Claim 2; further, the claimed sub-multiplication circuit recites features (multiplication by shifting) that correspond with subject matter treated above in the rejection of Claim 1 and are applicable hereto.

Claim 4 inherits all the limitations of Claim 2; further, the claimed sub-multiplication circuits recite features (inverters) that correspond with subject matter treated above in the rejection of Claim 1 and are applicable hereto.

Claim 5 inherits all the limitations of Claim 2; further, the claimed inverter circuit recites features (XOR) that correspond with subject matter treated above in the rejection of Claim 1 and are applicable hereto.

Claim 6 inherits all the limitations of Claim 2; further, Applicant's admitted prior art, Lemonds et al., and Tan et al., all fails to teach the use of an accumulator with a carry save adder device; however, Davis discloses a Booth multiplier and teaches an accumulation phase where the resultant partial products are formed and accumulated (col. 2, lines 31-32) and partial sum and carry save data for the sum of partial product (intermediate multiplication results) are produced (col. 2, lines 32-34); further, the final intermediate multiplication result is stored in an accumulator; and, in the final stage, the final partial sum and carry data is added together to produce the final multiplication result. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Davis into the method of Applicant's admitted prior art (in view of Lemonds et al. and Tan et al.) for producing the claimed invention because using the accumulator with a carry save adder device provides for generating and saving the sum and carry results of the final multiplication result.

Claim 7 inherits all the limitations of Claim 6; further, the claimed accumulator recites features (ripple adder device) that are well known techniques in the art for adding sum and carry results.

Claim 8 inherits all the limitations of Claim 7; further, the claimed ripple adder device recites features (receiving correcting bits) that are well known

techniques in the art needed for correcting the final result of an addition of two signed negative binary numbers.

Claim 9 inherits all the limitations of Claim 6; further, the claimed multiplier device recites features (register for storing filter output) that correspond with subject matter treated above in the rejection of claims 1 and 6 and are applicable hereto.

Claim 10 inherits all the limitations of Claim 2; further, the claimed multiplier device recites features (encoding a discrete digital level bit value) that correspond with subject matter treated above in the rejection of claims 1 and 2 and are applicable hereto.

Claim 11 inherits all the limitations of Claim 2; further, the claimed multiplier device recites features (the number is an error signal) that correspond with subject matter treated above in the rejection of claims 1 and 2 and are applicable hereto.

Claim 13 inherits all the limitations of Claim 12; further, the claimed method recites features (representing the 8 discrete digital level values in 8-VSB standards as a 3-bit code) that correspond with subject matter treated above in the rejection of claim 2 and are applicable hereto.

Claim 14 inherits all the limitations of Claim 13; further, the claimed method recites features (shifting bits to effect a multiplication of 4 or 8) that correspond with subject matter treated above in the rejection of claim 1 and are applicable hereto.

Claim 15 inherits all the limitations of Claim 13; further, the claimed method recites features (performing an inversion in the multiplication step) that correspond with subject matter treated above in the rejection of claim 1 and are applicable hereto.

Claim 17 inherits all the limitations of Claim 13; further, the claimed method recites features (storing a filter output result in a register and adding it with a final multiplication result) that correspond with subject matter treated above in the rejection of claims 1 and 6 and are applicable hereto.

As to **Claim 18**, the claimed multiplier recites features that correspond with subject matter mentioned above in the rejection of Claim 1 and are applicable hereto.

Claim 19 inherits all the limitations of Claim 18; further, the claimed method recites features that correspond with subject matter treated above in the rejection of claims 1, 2, and 3 and are applicable hereto.

Allowable Subject Matter

Claim16 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusions

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bhattacharya et al. [US 4782458] uses XOR gates for

inversion and multiplication by -1. Main [US 5402369] teaches the use of well-known carry ripple adder in a multiplier. Gitlin et al. [US 4924492] and Jiang [US 5958000] teach the need for a Booth multiplier and its implementation.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jamshid Goshtasbi-G., whose telephone number is (571) 272-3012. The examiner can normally be reached on M-F 8:00/4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel, can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jamshid Goshtasbi-G.
Examiner
Art Unit 2637

KHAI TRAN
PRIMARY EXAMINER 9/30/04